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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,355	09/19/2003	Jyh-Shiou Hsu	TS01-848	8187
7:	7590 03/08/2005		EXAMINER	
George O Saile 28 Davis Avenue			GOUDREAU, GEORGE A	
Poughkeepsie,		12603		PAPER NUMBER
			1763	
			DATE MAILED: 03/08/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
	10/666,355	HSU ET AL.	
Office Action Summary	Examiner	Art Unit	
	George A. Goudreau	1763	1.
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with th	ie correspondence a	address
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period of the period for reply within the set or extended period for reply will, by statute any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply by within the statutory minimum of thirty (30) will apply and will expire SIX (6) MONTHS, cause the application to become ABAND	ne timely filed) days will be considered tim from the mailing date of this ONED (35 U.S.C. § 133).	nely. : communication.
Status			
 1) ⊠ Responsive to communication(s) filed on (9-19) 2a) ☐ This action is FINAL. 2b) ⊠ This 3) ☐ Since this application is in condition for alloware closed in accordance with the practice under E 	action is non-final. nce except for formal matters,		he merits is
Disposition of Claims	•		
 4) Claim(s) 1-39 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) Claim(s) 26-39 is/are allowed. 6) Claim(s) 1-4,6-9 and 14-21 is/are rejected. 7) Claim(s) 5,10-13 and 22-25 is/are objected to. 8) Claim(s) are subject to restriction and/o 	wn from consideration.		
Application Papers			
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acc Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex	epted or b) objected to by t drawing(s) be held in abeyance. tion is required if the drawing(s) is	See 37 CFR 1.85(a). s objected to. See 37	CFR 1.121(d).
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Bureau	s have been received. s have been received in Appli rity documents have been rec	cation No	al Stage
* See the attached detailed Office action for a list	• • • • • • • • • • • • • • • • • • • •	eived.	
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) lnterview Sumn Paper No(s)/Ma 5) Notice of Inform 6) Other:	nary (PTO-413)	EXAMINER -05/ PTO-152)
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1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 9, 14-16, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Gardner et. al. (5,863,824).

Gardner et. al. disclose a process for gate (203) on a wafer which is comprised of the following steps:

- -A polysi gate electrode (203) on top of a pad oxide layer (205) are formed onto the surface of a Si wafer (201);
- -The gate is patterned.;
- -A first layer of oxide material is conformably formed onto the surface of the gate to form a type of first sidewall spacer (207) on the sides of the gate.;
- -The width of the first oxide sidewall spacer on the polysi gate is measured and compared against a targeted value.; and
- -A second Si3N4 sidewall spacer (209) is formed onto the sidewalls of the first spacer. The thickness of the second Si3N4 sidewall spacer is adjusted to compensate for any inaccuracies in the dimensions of the first SiO2 sidewall spacer formed onto the sides of the polysi gate.

This is discussed specifically in columns 4; and discussed in general in columns 1-6. This is shown in figures 1-3.

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3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 6-8, 17-19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the reference as applied in paragraph 2 above.

The reference as applied in paragraph 2 above fail to disclose the following aspects of applicant's claimed invention:

- -the specific dimensions for the spacer layers, and gate electrode width, which are claimed by the applicant; and
- -the specific method for forming the gate pad oxide layer which is claimed by the applicant

It would have been obvious to one skilled in the art to employ any of a variety of different methods for forming the gate pad oxide layer in the process, which is taught above including those, which are specifically claimed by the applicant. The usage of the specific means, which are claimed by the applicant for forming the gate pad oxide layer, is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for forming the gate pad oxide layer in the process taught above to the specific means, which are taught above.

It would have been obvious to one skilled in the art to form to form the spacer on the sidewalls of the gate electrode in the process taught above to the specific thickness Art Unit: 1763

gate electrode.

which are claimed by the applicant based upon the following. It would have been desirable to form spacers at a sufficient thickness that source, and drain implants can be formed at the proper distance from the sides of the gate electrode using the spacers as implant masks to prevent the implantation of the Si immediately adjacent the polysi

It would have been obvious to one skilled in the art to form the gate electrode to the specific width, which is claimed by the applicant based upon the following. It would have been desirable to form the gate electrode with a sufficient width to meet the current carrying needs of the gate electrode without forming the gate electrode with an excessive width, which would consume precious real estate on the chip to be fabricated.

- 5. Claims 5, 10-13, and 22-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 6. Claims 26-39 are allowed.
- 7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- 8. Any inquiry concerning this communication should be directed to examiner George A. Goudreau at telephone number (571)-272-1434.

George A. Goudrea Primary Examiner

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